Amendments to the Specification

Please enter the following amendments to the specification. These changes are simply to correct typographical errors and no new matter has been added.

Please replace paragraph **[0013]** beginning at page 5, line 11 with the following:

[0013] Therefore, there is a need for a system and method that can provide data integrity for modern storage systems that are operating in high band-[[with]] width environment.

Please replace paragraph **[0028]** beginning at page 8, line 5 with the following:

[0028] Figure 2A shows an adapter as used in a RAID controller, according [[tone]] to one aspect of the present invention;

Please replace paragraph **[0031]** beginning at page 8, line 14 with the following:

[0031] Figure 4 shows a block diagram of a system performing data integrity checks in the receive path, according to [[ne]] one aspect of the present invention;

Please replace paragraph **[0034]** beginning at page 8, line 23 with the following:

[0034] Figures 7A-7B show various register values that are used to perform data integrity tests, according to [[ne]] one aspect of the present invention.

Please replace paragraph **[0046]** beginning at page 11, line 8 with the following:

[0046] Figure 3 is a block diagram showing PCI interface 107 components, as used in the adaptive aspects of the present invention. PCI interface 107 includes direct memory access ("DMA") and arbitration logic and is operationally coupled to PCI bus 105 at one end and to fibre channel wire 311 at the other end. Frame Buffer ("FB") 308 is used to store information, when data moves from a host to storage system and vice-versa.

Please replace paragraph **[0049]** beginning at page 12, line 1 with the following:

[0049] PCI I/F 107 is also coupled to various other DMA units, for example, command DMA unit [[303]] 304, request DMA unit 303 and response DMA unit 302. These DMA units allow

the use of PCI I/F 107 to move information in and out of adapter 106 by using standard DMA techniques.

Please replace paragraph **[0055]** beginning at page 13, line 16 with the following:

[0055] CRC engine 401 generates the CRC 410, which is sent to CRC ACC register 403. Accumulated CRC values 402 and 402A are sent to processor 112 and CRC engine 401 respectively. CRC error 409, if any, is sent to processor 112, while CRC 402B is sent out via residue register 414 and PCI bus 105.